mobile phone or smart phone **2000** as shown in FIG. **33** or for a digital camera **3000** or a digital camcorder as shown in FIG. **34**.

**[0189]** Alternatively, the CMOS image sensor may be applied in a personal digital assistant (PDA), a portable multimedia player (PMP), a digital multimedia broadcast (DMB) device, a global positioning system (GPS), a handheld gaming console, a portable computer, a web tablet, a wireless phone, a digital music player, a memory card, or other electronic products, which may be configured to receive or transmit information data wirelessly.

**[0190]** According to exemplary embodiments of the inventive concept, a photoelectric conversion device (e.g., a photo diode) is realized using a doped epitaxial layer (e.g., of a first conductivity type) rather than an ion implantation process. In other words, the epitaxial layer may include pixel regions defined by a first device isolation layer, and an increased area of each pixel region can be used to generate photocharges from incident light as compared to a case in which ion implantation is used. In some exemplary embodiments, the whole area of each pixel region can be used to generate photocharges from incident light. The increase of a photocharge-generating area makes it possible to improve a full well capacity property of a CMOS image sensor. Thus, by using the CMOS image sensor according to exemplary embodiments of the inventive concept, it is possible to acquire more clear images.

**[0191]** In addition, since an ion implantation process for forming the photoelectric conversion device (e.g., a photo diode) can be omitted, it is possible to simplify a fabrication process of the CMOS image sensor and reduce a fabrication cost thereof.

**[0192]** Further, since the pixel regions are defined by a device isolation layer penetrating the epitaxial layer, it is possible to prevent a cross talk from occurring between the pixel regions.

**[0193]** Furthermore, a well impurity layer of a second conductivity type is formed in the epitaxial layer of the first conductivity type, and logic transistors are formed on the well impurity layer. Here, since the logic transistors can be overlapped with the photoelectric conversion device in a plan view, it is possible to fabricate a CMOS image sensor with an increased integration density.

**[0194]** While exemplary embodiments of the inventive concepts have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the attached claims.

What is claimed is:

**1**. A complementary metal-oxide-semiconductor (CMOS) image sensor, comprising:

an epitaxial layer having a first conductivity type and having a first surface and a second surface facing each other;

a first device isolation layer extending from the first surface to the second surface of the epitaxial layer to define a pixel region in the epitaxial layer;

a well impurity layer formed adjacent to the first surface and formed in the pixel region of the epitaxial layer, the well impurity layer having a second conductivity type;

a second device isolation layer formed adjacent to the first surface and formed in the well impurity layer to define a first active portion and a second active portion spaced apart from each other;

a charge transfer gate provided on the well impurity layer of the first active portion;

a floating diffusion region formed in the first active portion and beside the charge transfer gate; and

a logic transistor formed on the well impurity layer of the second active portion.

**2**. The CMOS image sensor of claim **1**, wherein the epitaxial layer comprises a first epitaxial layer having a first doping concentration, a second epitaxial layer having a second doping concentration different from the first doping concentration, and a third epitaxial layer having a third doping concentration different from the second doping concentration.

**3**. The CMOS image sensor of claim **2**, wherein the first epitaxial layer is adjacent to the second surface, the third epitaxial layer is adjacent to the first surface, and the second epitaxial layer is disposed between the first and third epitaxial layers, and

wherein the first doping concentration is lower than the second doping concentration, and the second doping concentration is lower than the third doping concentration.

**4**. The CMOS image sensor of claim **1**, wherein the first device isolation layer comprises an insulating layer extending from a bottom surface of the second device isolation layer to the second surface of the epitaxial layer, and the epitaxial layer is in direct contact with the device isolation layer.

**5**. The CMOS image sensor of claim **1**, further comprising a potential barrier layer having the second conductivity type and enclosing a sidewall of the first device isolation layer,

wherein a doping concentration of impurities of the second conductivity type is higher in the potential barrier layer than in the well impurity layer.

**6**. The CMOS image sensor of claim **1**, wherein the first device isolation layer comprises an insulating layer extending from a bottom surface of the second device isolation layer to the second surface of the epitaxial layer, and a width of the insulating layer increases in a direction from the first surface toward the second surface.

**7**. The CMOS image sensor of claim **1**, wherein the charge transfer gate has a bottom surface positioned at a lower level than that of a bottom surface of a gate electrode of the logic transistor.

**8**. The CMOS image sensor of claim **1**, further comprising a connection line electrically connecting the floating diffusion region to the logic transistor.

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